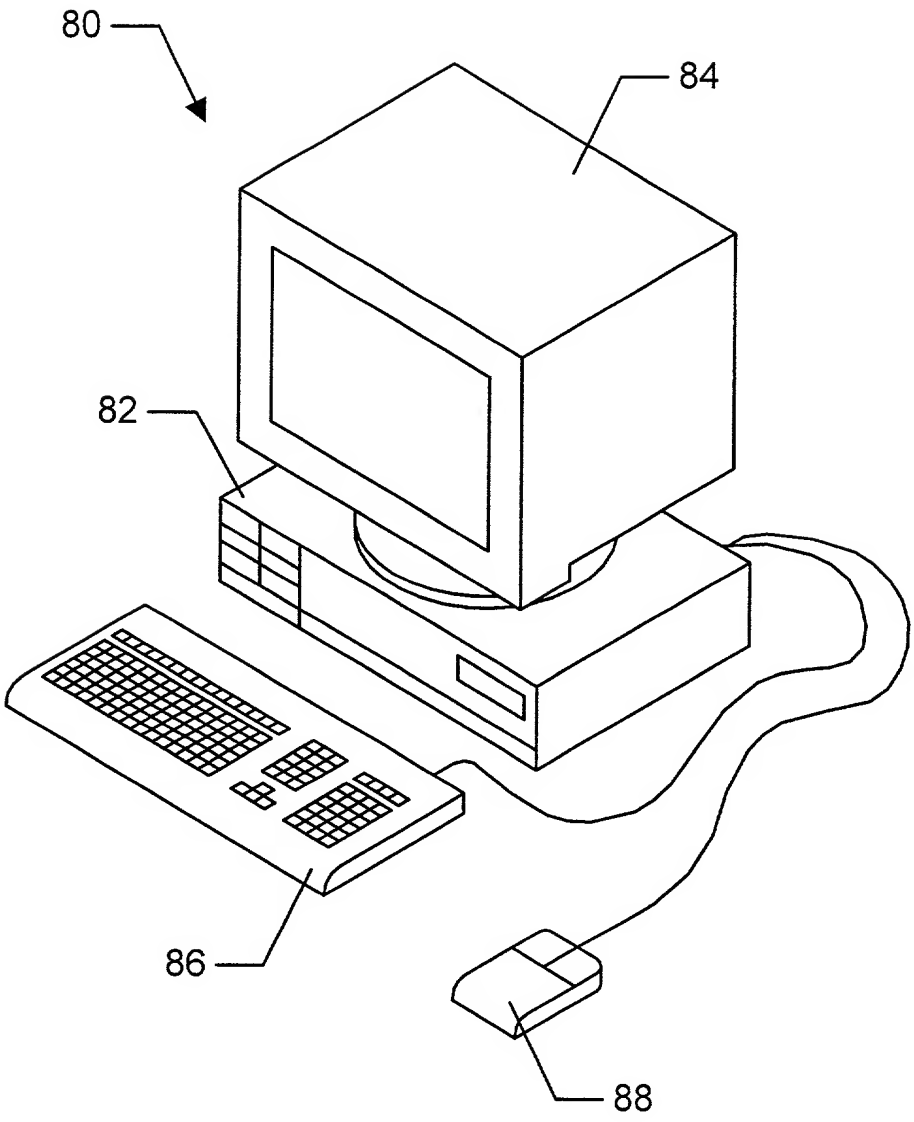


FIG. 1

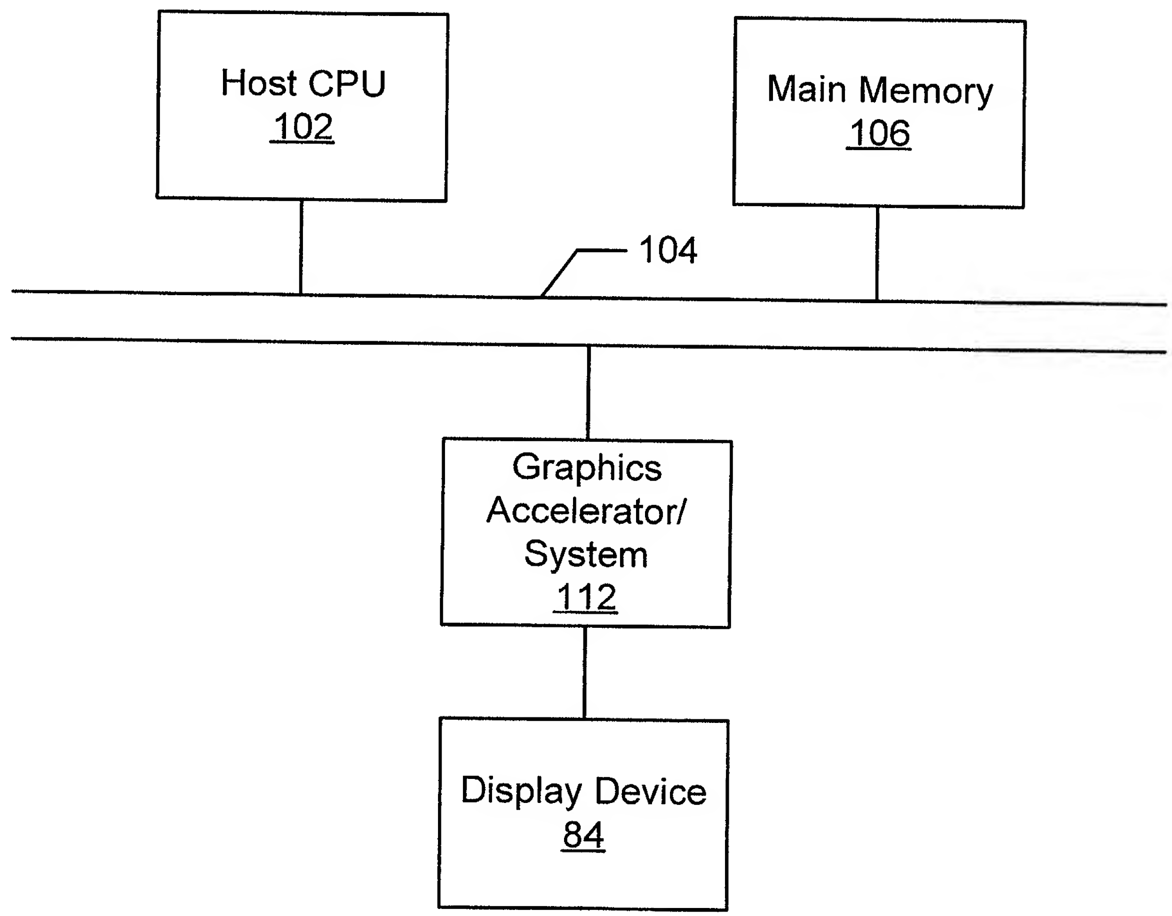

Host CPU
102
Main Memory
106
104
Graphics
Accelerator/
System
112
Display Device
84

FIG. 2

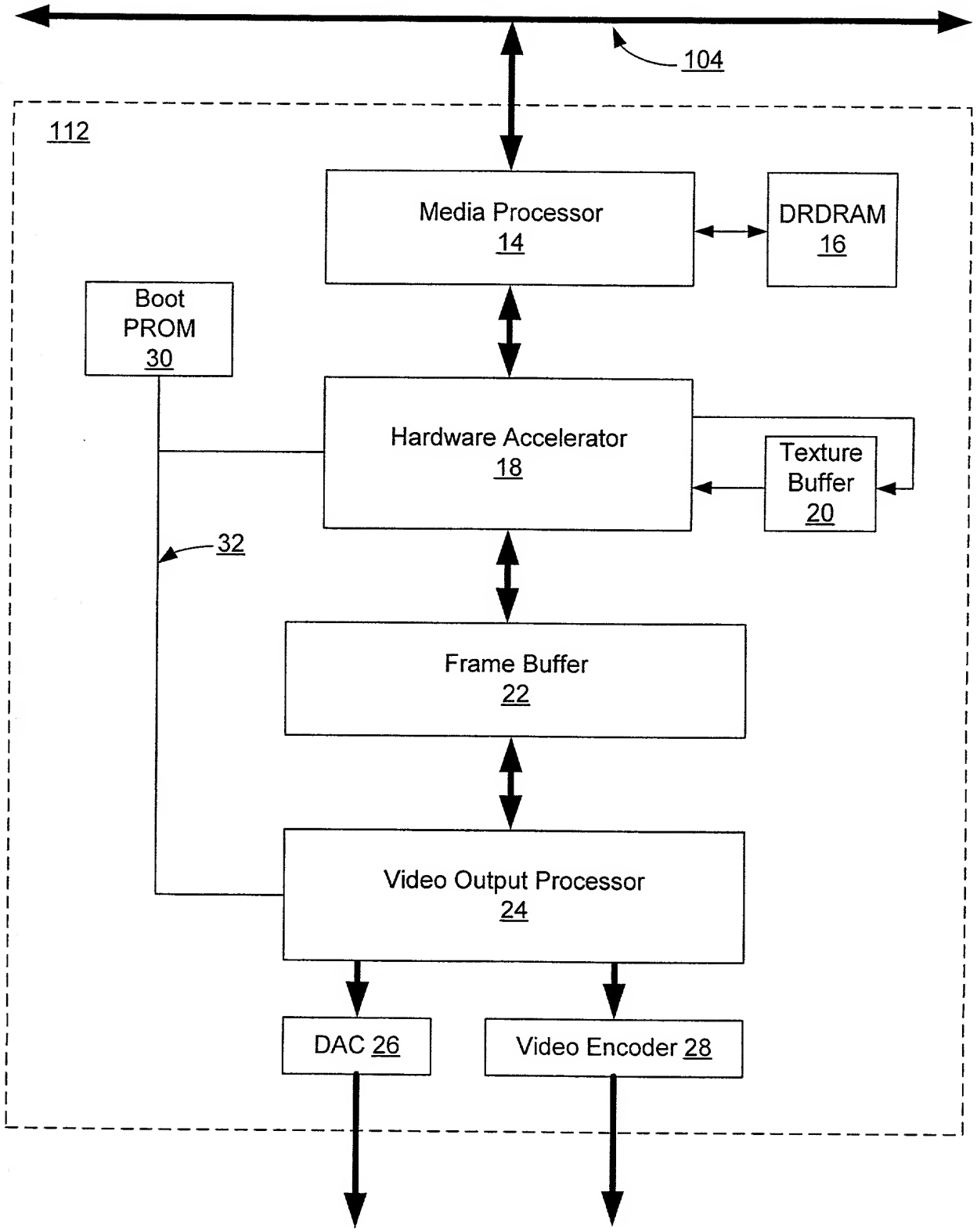

104
112
Media Processor
14
DRDRAM
16
Boot
PROM
30
Hardware Accelerator
18
Texture
Buffer
20
32
Frame Buffer
22
Video Output Processor
24
DAC 26
Video Encoder 28

FIG. 3

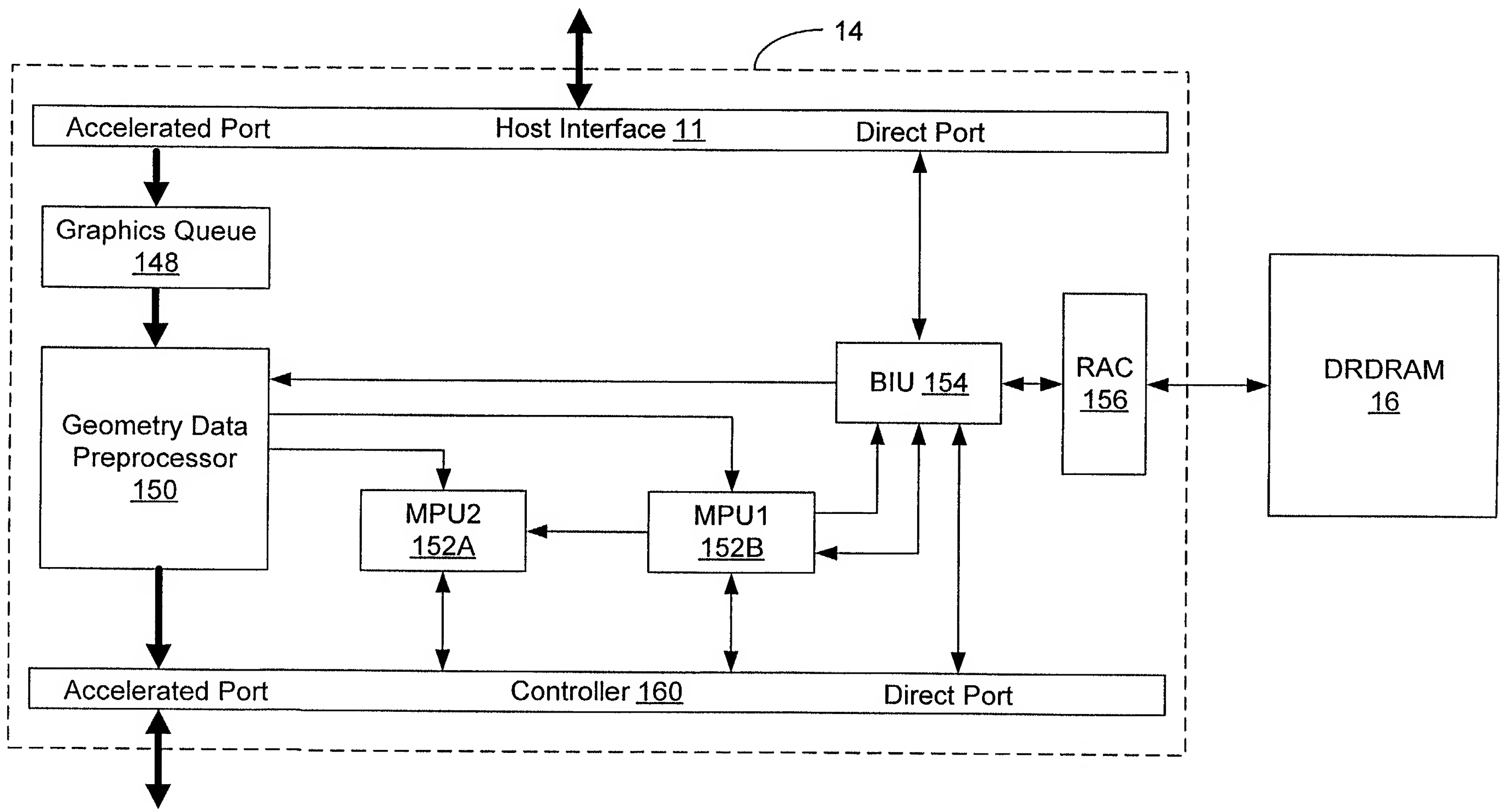

14
Accelerated Port
Host Interface 11
Direct Port
Graphics Queue 148
Geometry Data Preprocessor 150
BIU 154
RAC 156
DRDRAM 16
MPU2 152A
MPU1 152B
Accelerated Port
Controller 160
Direct Port

FIG. 4

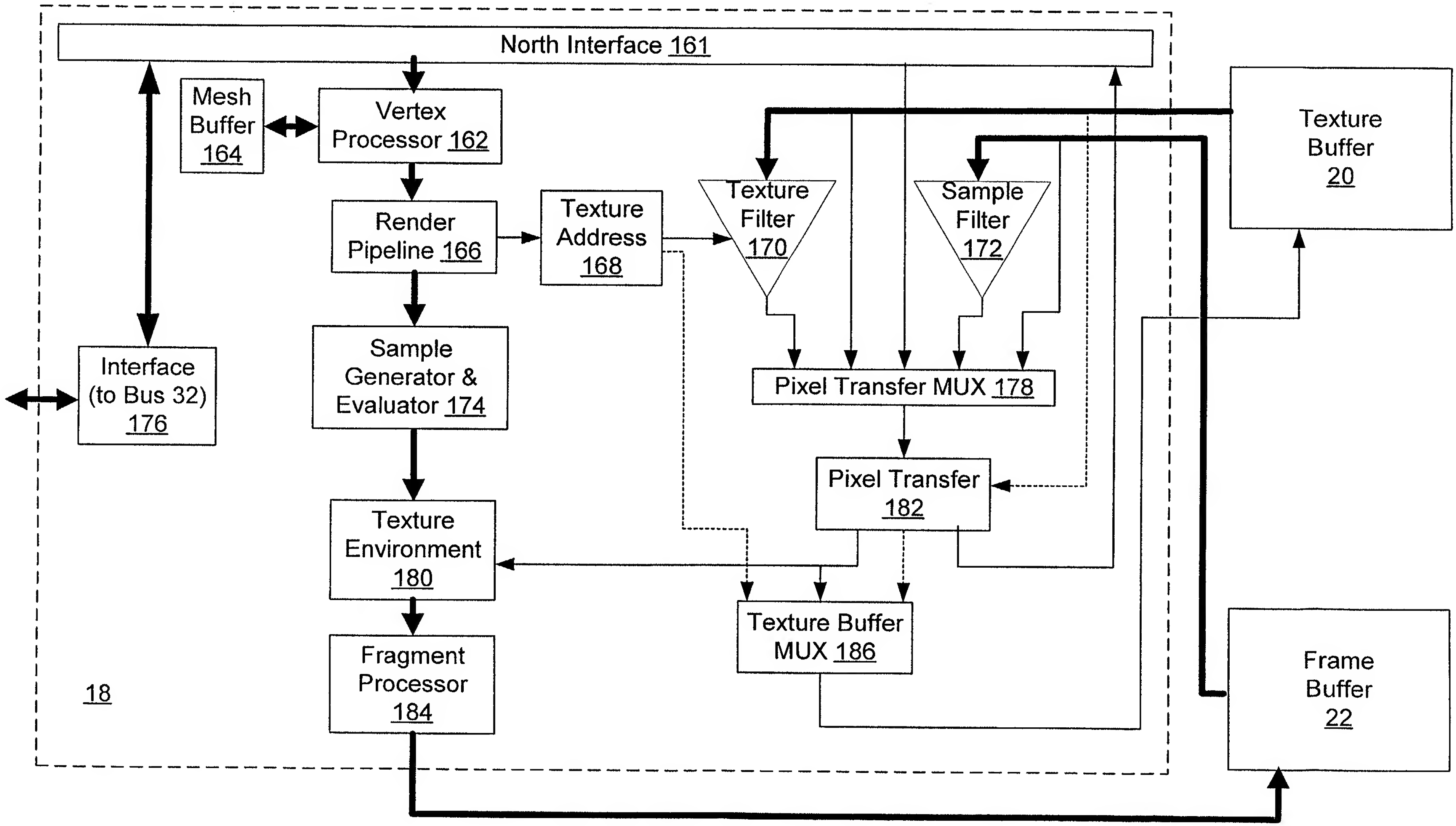
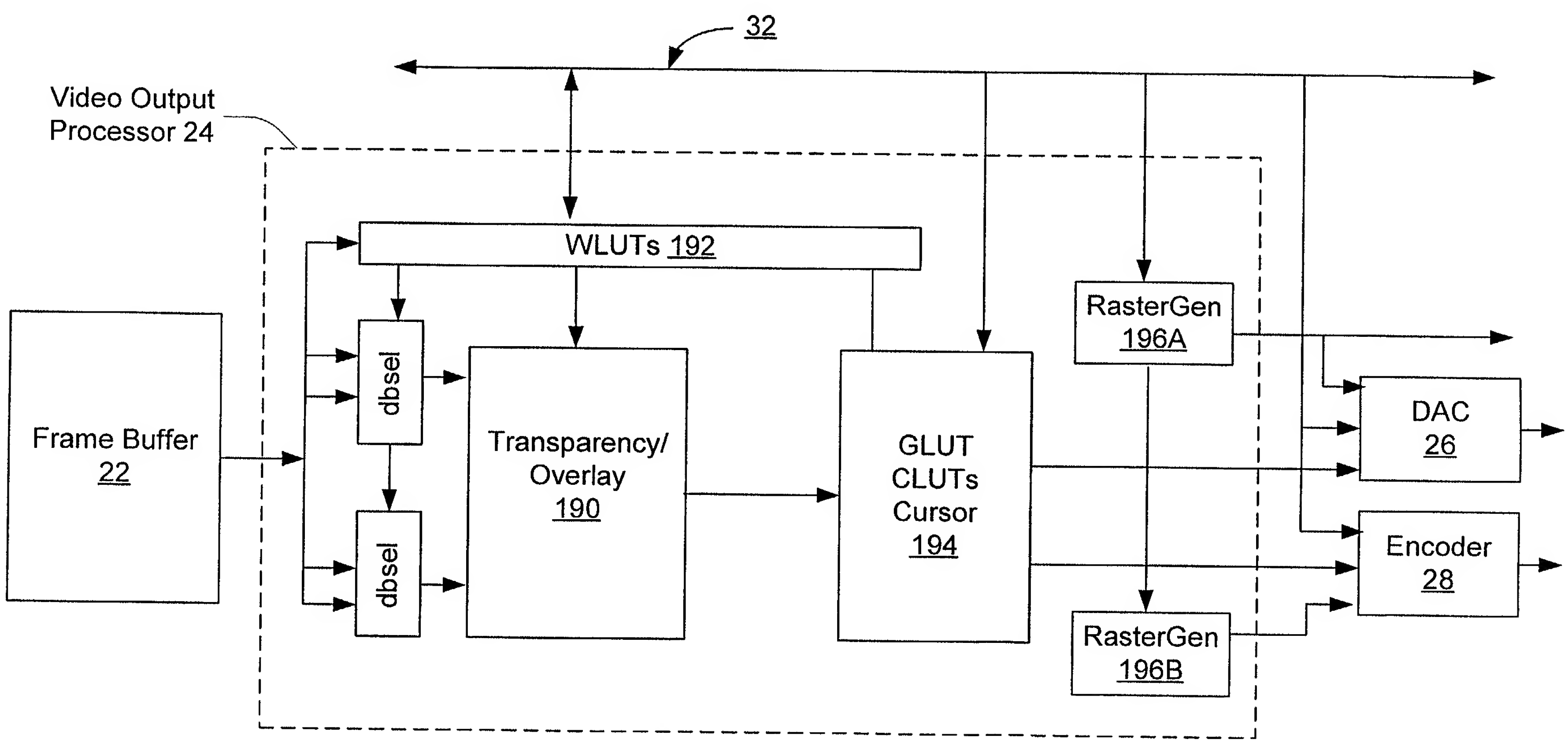

North Interface 161
Mesh Buffer 164
Vertex Processor 162
Render Pipeline 166
Texture Address 168
Texture Filter 170
Sample Filter 172
Texture Buffer 20
Interface (to Bus 32) 176
Sample Generator & Evaluator 174
Pixel Transfer MUX 178
Pixel Transfer 182
Texture Environment 180
Texture Buffer MUX 186
Fragment Processor 184
18
Frame Buffer 22

FIG. 5



32
Video Output
Processor 24
WLUTs 192
Frame Buffer
22
dbsel
dbsel
Transparency/
Overlay
190
GLUT
CLUTs
Cursor
194
RasterGen
196A
RasterGen
196B
DAC
26
Encoder
28

FIG. 6

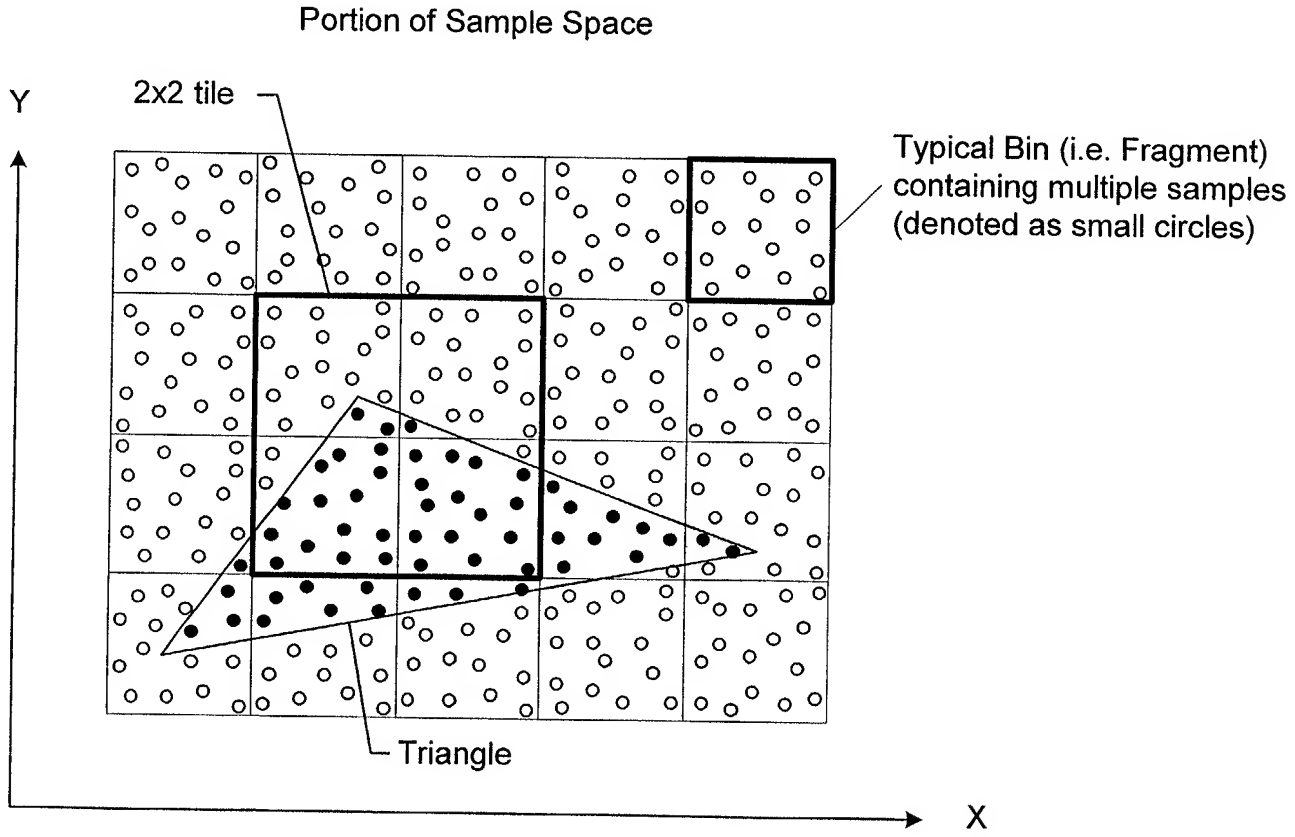

Portion of Sample Space
Y
2x2 tile
Typical Bin (i.e. Fragment)
containing multiple samples
(denoted as small circles)
Triangle
X

Fig. 7

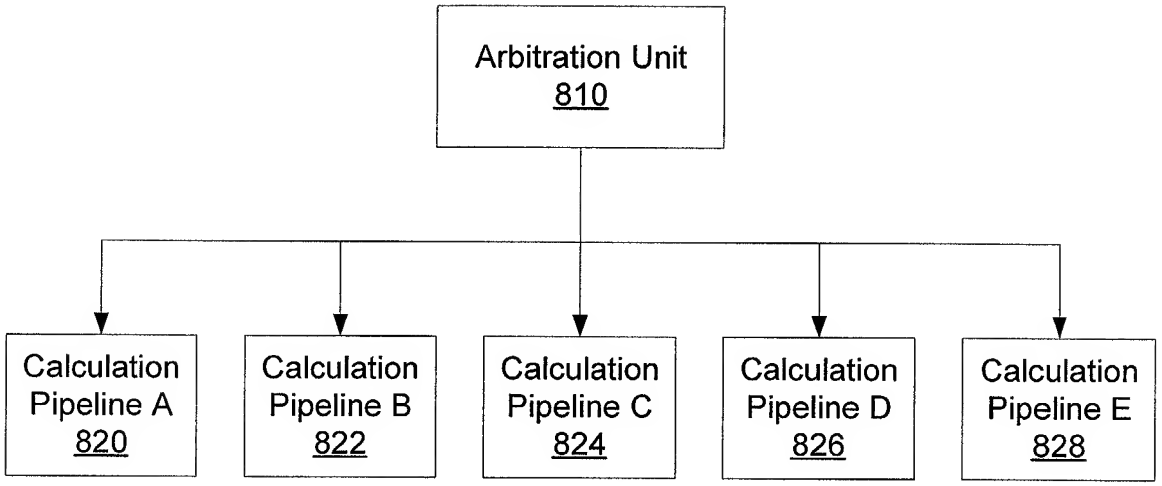

Arbitration Unit
810
Calculation Pipeline A
820
Calculation Pipeline B
822
Calculation Pipeline C
824
Calculation Pipeline D
826
Calculation Pipeline E
828

FIG. 8

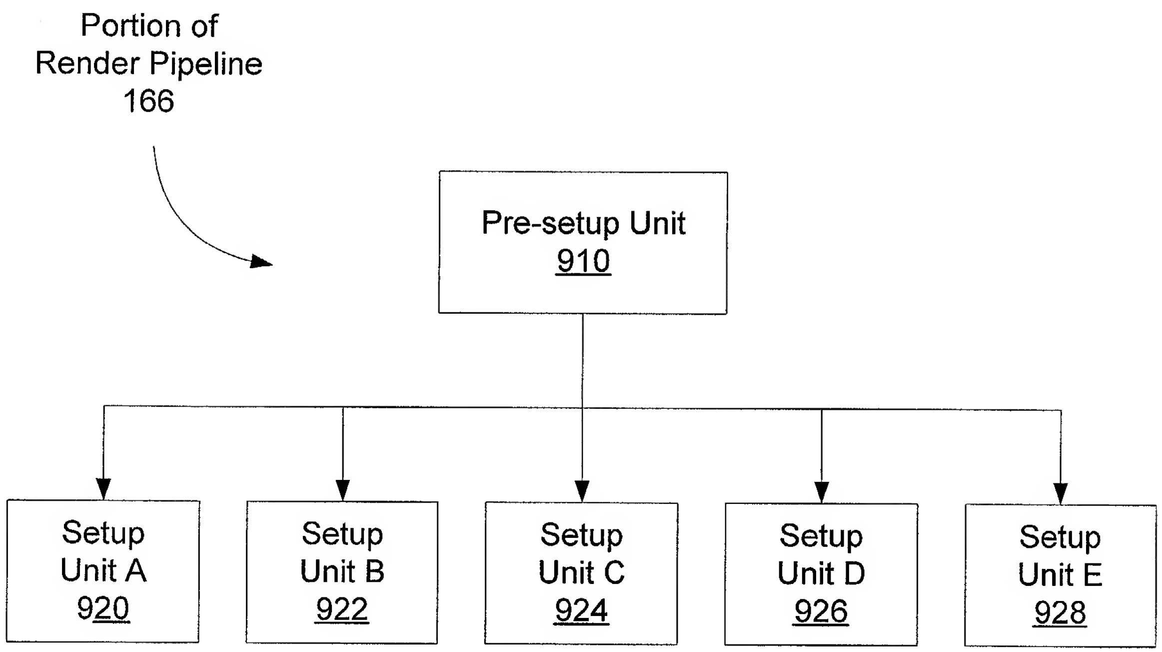

Portion of
Render Pipeline
166
Pre-setup Unit
910
Setup
Unit A
920
Setup
Unit B
922
Setup
Unit C
924
Setup
Unit D
926
Setup
Unit E
928

FIG. 9

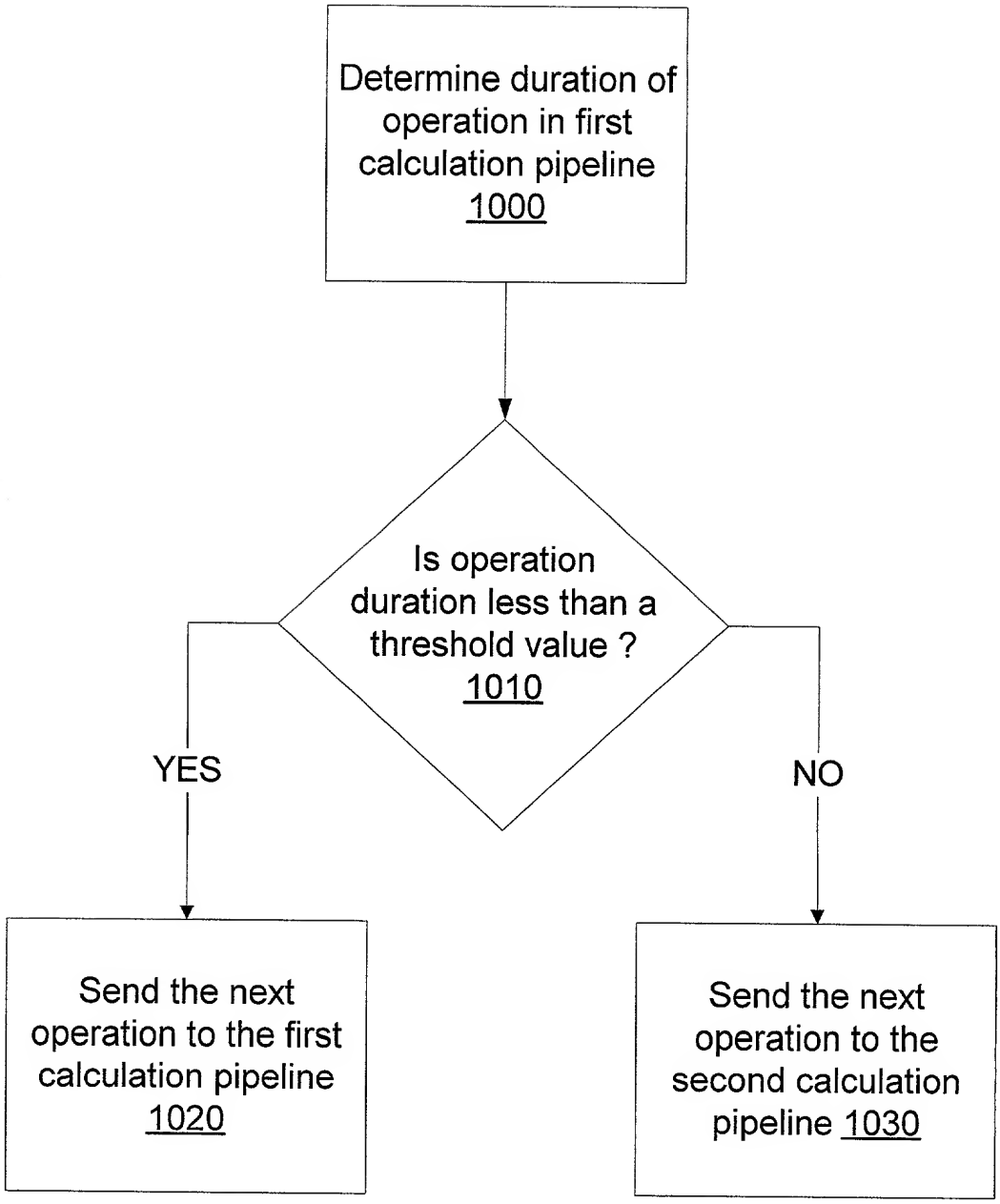

Determine duration of operation in first calculation pipeline 1000
Is operation duration less than a threshold value ? 1010
YES
NO
Send the next operation to the first calculation pipeline 1020
Send the next operation to the second calculation pipeline 1030

FIG. 10